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EXAMINER

DAO, THUY CHAN

ART UNIT

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PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/009,649	Applicant(s) VORBACH ET AL.	
	Examiner Thuy Dao	Art Unit 2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 30 October 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 179-181 and 183-203 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 179-181 and 183-203 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 29 May 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>01/12/09</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This action is responsive to the amendment filed on October 30, 2008.
2. Claims 179-181 and 183-203 have been examined.

Response to Amendments

3. In the instant amendment, claims 179-181, 186, 190, 194 and 203 have been amended.
4. The objection to claim 203 is withdrawn in view of Applicant's amendments.

Specification

5. The abstract of the disclosure does not commence on a separate sheet in accordance with 37 CFR 1.52(b)(4).

As acknowledged by the Applicants (Remarks, page 7), a replacement Abstract was filed on September 28, 2006. In this amendment, page 2 includes the replacement Abstract and other amendments of the specification.

Accordingly, a new abstract of the disclosure is required and must be presented on a separate sheet, apart from any other text.

Response to Arguments

6. Applicants' arguments have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections – 35 USC §102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application

filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 179-181 and 183-189 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. 5,801,958 (art made of record, hereafter "Dangelo").

Claim 179:

Dangelo discloses *a method for programming a system having a configurable cellular structure, comprising:*

extracting a control flow graph of a program (e.g., col.71: 50 – col.72: 49; col.73: 27-55; col.75: 4-67);

separating the control flow graph into a plurality of subgraphs (e.g., col.17: 59 – col.18: 26-37; col.28: 26-54; col.61: 7-34);

distributing the plurality of subgraphs among a plurality of programmable hardware modules; determining state information for each of the subgraphs (e.g., col.62: 6-27; col.17: 60 – col.18: 57; col.16: 37-59; col.17: 54-67); and

transferring the state information determined for one of the subgraphs from the one of the subgraphs to a subsequently executed subgraph (e.g., col.31: 1-36; col.54: 49 col.55: 2; col.39: 29-45; col.57: 26-35).

Claim 180:

Dangelo discloses *a method for programming a system having a configurable cellular structure, comprising:*

extracting a data flow graph of a program that includes a loop (e.g., FIG. 25b, col.38: 58-65; col.79: 22-48; FIG. 36g, col.82: 1-32; FIG. 36f, col.81: 52-57);

separating the data flow graph into a plurality of subgraphs, such that the loop is split into several of the subgraphs (e.g., col.48: 1-40; col.62: 6-27); and

distributing the plurality of subgraphs among a plurality of hardware modules such that, the several of subgraphs of the loop are distributed among at least two of the hardware modules (e.g., col.82: 1-42; col.52: 2-44; FIG. 1, ASIC chip 110; col.16: 51-58; col.62: 6-32; col.33: 46-61; FIG. 20b, multi-chip module 2000).

Claim 181:

Dangelo discloses *a method for programming a system having a cellular structure, comprising:*

extracting from a program at least one of a data flow graph and a control flow graph (e.g., FIG. 25b, col.38: 57-65; col.69: 1-5; col.72: 3-14);

separating the at least one of the graphs into a plurality of subgraphs (e.g., col.26: 15-31; col.35: 27-29; col.52: 15-39); and

distributing the plurality of subgraphs among a plurality of hardware modules (e.g., col.33: 1-45; col.34: 43-50; col.17: 8-24);

wherein the separating includes providing communication arrangements adapted for storage separating the at least one of all data to be processed (e.g., col.15: 38-62; col.75: 4-40)

in a subsequent hardware module according to connections between the between the plurality of subgraphs (e.g., col.20: 45-61; col.5: 1-27; col.9: 46-67; col.29: 20-42).

Claim 183:

Dangelo discloses *the method of claim 181, wherein the separating includes separating the at least one the graphs into the plurality of subgraphs so that data transmission between the plurality of subgraphs is minimized (e.g., col.17: 44-67; col.59: 63 – col.60: 16).*

Claim 184:

Dangelo discloses *the method of claim 181, wherein the separating includes separating the at least one of the graphs into the plurality of subgraphs so that no loop-back is obtained between the plurality of subgraphs (e.g., col.39: 29-45; col.82: 1-33).*

Claim 185:

Dangelo discloses *the method of claim 181, wherein the separating includes separating the at least one of the graphs into the plurality of subgraphs so that the subgraphs match resources of the hardware modules (e.g., col.18: 5-12; col.19: 1-16).*

Claim 186:

Dangelo discloses *the method of claim 181, wherein memory elements are inserted between the plurality of subgraphs, the memory elements adapted to save data passed between subgraphs (e.g., col.62: 48-66; col.71: 1-14; FIG. 25c and related text).*

Claim 187:

Dangelo discloses *the method of claim 181, wherein each of the plurality of subgraphs includes nodes, the method further comprising: transmitting status signals between nodes within one of the subgraphs so that a state of each individual one of the nodes of the one of the subgraphs is available to each of the other nodes of the one of the subgraphs (e.g., col.30: 25-49; col.31: 1-30; col.26: 15-32; col.74: 15-24).*

Claim 188:

Dangelo discloses *the method of claim 181, wherein each of the plurality of subgraphs includes nodes, the method further comprising: transmitting status signals from a first node of at least one of the plurality of subgraphs to a higher-level unit adapted to control configuration of the plurality of hardware modules so as to trigger reconfiguration (e.g., 2: 44-56; col.5: 28-47).*

Claim 189:

Dangelo discloses *the method of claim 181, wherein the extracting includes, for a conditional instruction, extracting a plurality of different subgraphs, each representing a different instruction path, one of the different subgraphs being executed depending on an evaluation of the conditional instruction (e.g., col.75: 42-54; col.78: 16-65; col.80: 3-40).*

9. Claims 194-202 are rejected under 35 U.S.C. 102(b) as being anticipated by Getzinger (art made of record, US Patent No. 4,972,314).

Claim 194:

Getzinger discloses *a method of executing a program on a runtime reconfigurable array of cells* (e.g., FIG. 1, Parallel Processing Concept with 16 Arithmetic Processors 1-16, col.5: 64 – col.6: 14), *the method comprising:*

forming a plurality of subgraphs based on a program (e.g.,

FIG. 1, Graph Process Controller, col.4: 63-67; a plurality of subgraphs as node structures, col.9: 37-48;

node instances (subgraph instances) are ready to “independently and concurrently” executed by placing them on a dispatch queue, col.11: 60-67 and col.1: 52-59;

nodes (subgraphs) are scheduled and dispatched to 16 Arithmetic Processors AP 1-16, col.16: 65 – col.17:21 and FIG. 1);

computing a first part of a first one of the subgraphs with a first cell (e.g., FIG. 5, Graph {A, B, C}, first subgraph as {A, C}, second subgraph as {B}, col.9: 36-62; first part A of first subgraph {A, C} computed with a first Arithmetic Processor AP 1);

after the computing, reconfiguring the first cell for computation of a first part of a second one of the subgraphs (e.g., FIG. 5, after the computing, reconfiguring AP 1 for computation first part B of second subgraph {B}, please see Node A output source to 2, 2 sink to B, B assigned to AP 1); *and*

simultaneously with the reconfiguring, computing a second part of the first subgraph with a second cell (e.g., FIG. 5, simultaneously, computing second part C of first subgraph {A, C} with a second Arithmetic Processor AP 2, please see more in FIG. 3 with Dispatch Queue, Arithmetic Processors (in the instant case: 2 APs), Graph Process Controller GPC Scheduler, col.11: 60 - col.12: 29);

wherein state information determined for one of the subgraphs is transferred from the one of the subgraphs to a subsequently executed subgraph (e.g.,

FIG. 7 and related text; FIG. 39, current node ID --> fetch node instances --> executive primitive --> load subsequent node; FIG. 47, transferring data, status and signal).

Claim 195:

The rejection of base claim 194 is incorporated. Getzinger also discloses *storing configurations for the first one of the subgraphs and the second one of the subgraphs configuration registers associated with the first cell* (e.g., FIG. 9, Graphic Processor Memory GPM, col.17: 22 - 59).

Claim 196:

The rejection of intervening claim 195 is incorporated. Getzinger also discloses *marking unconfigured ones the configuration registers as unconfigured* (e.g., col.28: 48 – col.29: 36).

Claim 197:

The rejection of base claim 194 is incorporated. Getzinger also discloses *selecting a configuration for the first cell based on a status signal generated by the cell structure* (e.g., FIG. 3, col.11: 60 – col.12: 30).

Claim 198:

The rejection of base claim 194 is incorporated. Getzinger also discloses *selecting a configuration for the first cell based on a status signal generated by a higher-level loading unit* (e.g., FIG. 2, col.7: 22 – col.8: 29).

Claim 199:

The rejection of base claim 194 is incorporated. Getzinger also discloses *selecting a configuration for the first cell based on an externally generated status signal* (e.g., FIG. 2, col.7: 22 – col.8: 29).

Claim 200:

The rejection of base claim 194 is incorporated. Getzinger also discloses *selecting a configuration for the first cell as a function of a present configuration of the first cell and a received status signal* (e.g., FIG. 3, col.11: 60 – col.12: 30).

Claim 201:

The rejection of base claim 194 is incorporated. Getzinger also discloses:
activating an unconfigured configuration register in the first cell (e.g., col.28: 48 – col.29: 36);
requesting a configuration from a higher-level load unit when the unconfigured configuration register is activated (e.g., col.7: 22 – col.8: 29); and
suspending execution of a subgraph until the requested configuration is fully loaded (e.g., FIG. 7, Graph Process Controller Functions, col.14: 31-66).

Claim 202:

The rejection of base claim 194 is incorporated. Getzinger also discloses *triggering a loading of a configuration of the first cell when a status signal generated by the cell structure received by the first cell* (e.g., col.9: 11-28).

Claim Rejections – 35 USC §103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

11. Claims 190-193 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dangelo in view of US Patent No. 6,421,808 to McGeer et al. (art made of record, hereafter "McGeer").

Claim 190:

Dangelo discloses *a method of executing a single program on a system having an array of runtime reconfigurable cells, comprising:*

separating the single program into several subgraphs (e.g., col.17: 17-43; col.26: 15-46; col.47: 50-67; col.52: 15-39);

distributing the several subgraphs among different cells of the array (e.g., col.17: 54 – col.18: 37; col.21: 45-67); and

executing the several subgraphs via the cells, the executing including: transmitting a data signal from a first cell via which a first one of the subgraphs is executed to a second cell via which a second one of the subgraphs is executed.

Dangelo does not explicitly disclose *transmitting a status with the data signal, the status indicating whether the data signal is valid.*

However, in an analogous art, McGeer further discloses *transmitting a status with the data signal, the status indicating whether the data signal is valid (e.g., col.13: 59-67; col.14: 64 – col. 15: 12; col.30: 66 – col.31: 16; col.31: 44-67).*

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine McGeer's teaching into Dangelo's teaching. One would have been motivated to do so to perform computation based on valid input signals as suggested by McGeer (e.g., col.3: 26-57).

Claim 191:

McGeer discloses *the method of claim 190, further comprising: receiving a valid data signal at the second cell; and acknowledging receipt of the valid data signal (e.g., col.15: 43 – col.16: 59).*

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine McGeer's teaching into Dangelo's teaching. One would have been motivated to do so to as set forth above.

Claim 192:

Dangelo discloses *the method of claim 191, further comprising, transmitting by the second cell an indication that a signal is expected* (e.g., col.16: 9-16; col.19: 50 – col.20: 57).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine McGeer's teaching into Dangelo's teaching. One would have been motivated to do so to as set forth above.

Claim 193:

Dangelo discloses *the method of claim 192, further comprising: transmitting by the first cell an indication that the first cell is transmitting the expected signal* (e.g., col.15: 43 – col.16: 59; col.16: 9-16; col.19: 50 – col.20: 57).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine McGeer's teaching into Dangelo's teaching. One would have been motivated to do so to as set forth above.

12. Claim 203 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. Dangelo in view of US Patent No. 6,708,325 to Phillips et al. (art made of record, hereafter "Phillips").

Claim 203:

Dangelo discloses *a method for programming a system having a runtime configurable cellular structure, comprising:*

extracting from a program at least one of a data flow graph and a control flow graph (e.g., FIG. 25b, col.38: 57-65; col.69: 1-5; col.73: 27-55);

separating the at least one of the graphs into a plurality of subgraphs (e.g., col.17: 60 – col.18: 37; col.21: 45 – col.22: 37); and

distributing the plurality of subgraphs among a plurality of hardware modules (e.g., col.62: 6-27; col.26: 1-31); *wherein:*

the extracting includes, for a conditional instruction of the program, extracting a plurality of different subgraphs (e.g., col.78: 1-39; col.80: 3-44),

the distribution of the plurality of subgraphs includes adapting the plurality of hardware modules such that state information determined for a first one of the subgraphs is transferred from the first one of the subgraphs to another subgraph that is to be subsequently executed (e.g., col.54: 65 – col.55: 2; col.61: 7-33; col.31: 1-36; col.71: 1-12).

Dangelo does not explicitly disclose other limitations. However, in an analogous art, Phillips further discloses:

extracting a plurality of different subgraphs, each representing a different instruction path of the conditional instruction (e.g., col.6: 23-67),

the conditional instruction indicating which of the executed instruction paths is to be selected for providing output of the selected instruction path output to a further subgraph (e.g., col.3: 66 – col.4: 35; col.7: 47 – col.8: 19);

for each one of the different subgraphs, the system sets execution of the subgraph to be bypassed as soon as an evaluation in accordance with the conditional instruction reveals that output of the subgraph will not be selected (e.g., col.8: 9-19).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine Phillips' teaching into Dangelo's teaching. One would have been motivated to do so to perform branch prediction and to load the actually needed configuration in the case of missed prediction as suggested by Phillips (e.g., col.8: 9-19).

Conclusion

13. Applicants' amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

14. Any inquiry concerning this communication should be directed to examiner Thuy Dao (Twee), whose telephone/fax numbers are (571) 272 8570 and (571) 273 8570, respectively. The examiner can normally be reached on every Tuesday, Thursday, and Friday from 6:00AM to 6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam, can be reached at (571) 272 3695.

The fax phone number for the organization where this application or proceeding is assigned is (571) 273 8300.

Any inquiry of a general nature of relating to the status of this application or proceeding should be directed to the TC 2100 Group receptionist whose telephone number is (571) 272 2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Thuy Dao/
Examiner, Art Unit 2192

/Tuan Q. Dam/
Supervisory Patent Examiner, Art Unit 2192